

our work, we are *recycling* the imbalance to maintain the output node within a certain tolerance limit. By using a switched-capacitor regulator, the current efficiency can be more than 100% unlike for a linear regulator. This idea is an extension of the work on GALS stacked cores, which allows the intermediate node to implicitly track the workloads [3].

III. SWITCHED-CAPACITOR REGULATOR

In order to recycle the imbalance between the cores, current needs to be either sourced or sinked, depending on which core consumes more current. When the top core consumes more the regulator needs to *sink* current, while it needs to *source* current when the bottom core consumes more. The regulator style chosen for this design is a modified version of a conventional switched-capacitor circuit (Fig. 2). The design is implemented with four capacitors and eight switches [3]. Extremely interesting is that, unlike in conventional push-pull designs, with such a switched-cap solution the *sinked* current is *fed back* to the top core, thus reducing power waste. The two *flying* capacitors change roles periodically, providing the source/sink of charges. To understand how the circuit works, consider an example with a slightly imbalanced workload, where the current offset pushes V_{mid} to droop below half- V_{dd} . In the first phase, as the voltage droops down at the load, capacitor C_{SW1} begins charging to a voltage above half- V_{dd} , while the voltage on C_{SW2} falls below half- V_{dd} . In the second phase, through the on-chip switches, the capacitors C_{SW1} and C_{SW2} switch places. Since the voltage on C_{SW1} was charged to a higher voltage, it redirects this charge back onto the larger capacitor C_{D2} . This redirection of charge helps pull the load voltage back towards half- V_{dd} .

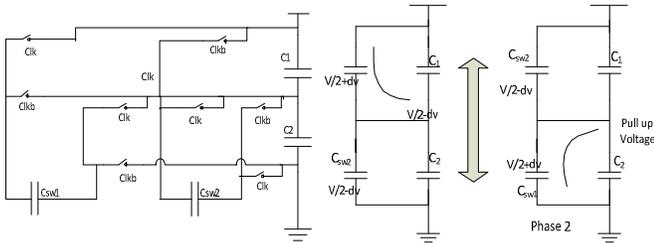


Fig2. Switched-Capacitor Regulator (left) and the two operational phases of the switched-capacitor (right). Phase1 shows the voltage decreasing at the load; during phase2 this charge is redirected back to the load through the fly-cap C_{sw2}

One of the primary loss components in a switched-capacitor regulator is the switching loss due to the power switches. For a conventional DC-DC converter providing current to parallel cores, the entire current needs to flow through the regulator causing large IR drop, thus reducing efficiency. However, in our technique of down conversion, most of the current is recycled from the top core and only the *difference* of the current imbalance needs to flow through the regulator (Fig 3). This accounts for a high efficiency for stacked DC-DC conversion.

IIIA Regulator Design Rules

The periodic swapping of the fly caps (C_{sw1} , C_{sw2}) with switching frequency (T_{sw}) causes the mid voltage (V_{mid}) to

jump between V_{max} and V_{min} . The p-p ripple (ΔV) on V_{mid} sets the design constraints for the regulator.

$$\Delta V = \frac{I_{diff} T_{sw}}{C_{sw}} \quad (2)$$

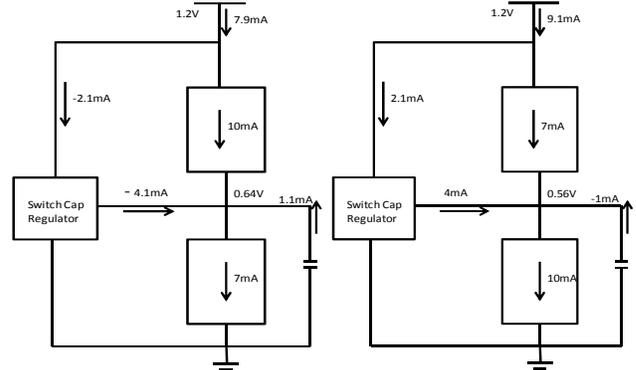


Fig. 3 Excess current between the stacked domains being sourced by the regulator (left) or fed back to the top core following Kirchoff's law (right)

The current consumption of the 2 cores is given by:

$$I_{top} = \alpha_{top} C_L (V_{dd} - V_{mid}) F_c \quad I_{bottom} = \alpha_{Bottom} C_L V_{mid} F_c \quad (3)$$

Replacing $I_{diff} = I_{top} - I_{bottom} = (\alpha_{top} V_{dd} - \alpha_{top} V_{mid} - \alpha_{Bottom} V_{mid}) C_L F_c$ in (2) we get:

$$\Delta V = \frac{K C_L T_{sw}}{C_{sw} T_c} \quad (4)$$

Where $K = \alpha_{top} V_{dd} - \alpha_{top} V_{mid} - \alpha_{Bottom} V_{mid}$, C_L denotes the capacitive load and T_c the core frequency.

Thus for a given imbalance, in order to reduce the ripple margin, $C_{sw} > C_L$ and switching frequency (F_{sw}) > core frequency (F_c) are necessary. Large capacitances incur high bottom-plate loss [6] as well as area cost whereas switching frequency is directly proportional to loss. Another major loss component that needs to be optimized involves the switches. The RC time constants which are formed between the switches and C , must be smaller than T_{sw} . Based on the above mentioned design rules, sensitivity analysis has been done to select the optimized R, C and switching frequency (F_{sw}) (Fig 4).

IIIB Open-Loop versus Close-Loop Regulation

In conventional DC-DC converter, open-loop system will typically have lower efficiency than close-loop system as the close-loop feedback path can try to modulate switching frequency/switch conductance in accordance with V_{out} , thus reducing the losses. However stacked-cores unlike conventional have an inherent self-regulation [5] as explained below. By charge conservation $I_{top} = I_{bottom}$

$$\text{Using Eq 3, } V_1 = V_{dd} - V_{mid} = \frac{\alpha_{Bottom}}{\alpha_{Top} + \alpha_{Bottom}} V_{dd} \\ V_2 = V_{mid} = \frac{\alpha_{Top}}{\alpha_{Top} + \alpha_{Bottom}} V_{dd} \quad (5)$$

If the core activity factors and core frequency are similar, V_{mid} will settle around half V_{dd} . Thus there is an inherent feedback loop in the system that forces the voltage headroom to be lower for the core that demands higher current, hence acting against the notion of DVS. In order to overcome this natural

feedback loop, the push-pull switched-capacitor is needed to regulate the V_{mid} . Going by general convention, closing this open loop regulator should improve efficiency. In this work, we have designed a hysteresis loop based feedback scheme that modulates the switching frequency in accordance with V_{out} .

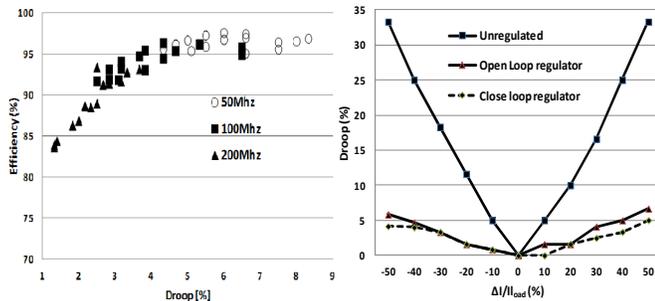


Fig4. Sensitivity Analysis for R, C and F_c

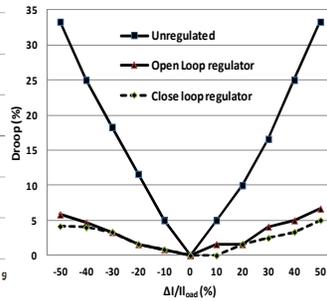


Fig5. Mid rail droop versus regulation scheme

The feedback path consists of 2 comparators along with a logic block that increases or decreases the regulator frequency as the upper or lower boundary (allowable droop margin) is crossed. Fig 5 shows the amount of droop ($\Delta V_{out}/V_{out}$) on the V_{mid} node for varying imbalance between the top and bottom core. The more the imbalance, the more the self-regulation of the system will force the V_{mid} node to go in the opposite direction as seen from the unregulated stacked mid rail. The push-pull scheme is thus essential to maintain balance. Closing the feedback loop improves the droop but at the cost of efficiency as seen from the Fig 6. This loss is coming from the design overhead that comes in the feedback path. At an imbalance of 50%, by using a close-loop switched-capacitor regulator, droop improves by 1.67% while suffering an efficiency loss of 14% over open loop regulation. Thus unlike conventional open-loop regulators, stacked voltage domain with its self-regulation will work at higher energy efficiency with open loop regulation. This technique down converts 1.2V-0.6V at 10mA load current with an efficiency of 90-93% even under workload difference of 50% between the cores. At 100% workload difference, it will work as a conventional switched-cap regulator with efficiency of 65-70%. Thus careful monitoring and allocation of core workload will allow high efficiency in this technique of DC-DC conversion [5].

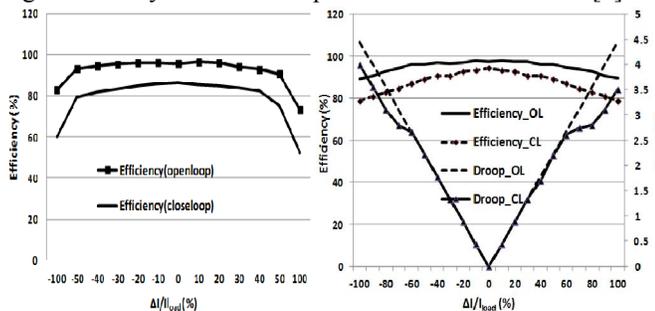


Fig6. 2:1 conversion efficiency with varying imbalance (10mA I_{load} , $V_{dd}=1.2V$)

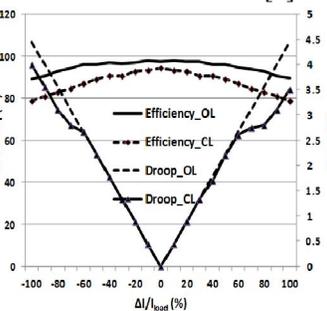


Fig7. Overheads of Sub/Near- threshold DC-DC Conversion (OL-Open Loop, CL-Close loop)

One of the primary aims of our work is to convert high off chip voltage to near threshold voltage at higher efficiency. Existing state of art techniques [6] measure efficiencies close to 70% across various I_{load} . Thus the achievable energy gain by using sub/near threshold V_{dd} decreases by 30%. To show the usefulness of stacked DC-DC conversion, we have scaled down our circuit to generate near threshold voltages. Fig 7 shows 90% conversion efficiency for 0.9v-0.45V at I_{loads} of 200-300uA for current imbalance between cores as high as 70-80%. Even at a 100% imbalance where the switched-capacitor regulator provides the entire current to one of the core while the other one is off, efficiency remains high (~85%). This is mainly because conventional power delivery, unlike stacked power delivery cannot work in open loop and the feedback circuitry incurs the additional losses.

IV. CONCLUSION

In this work, we have exploited the concept of charge recycling through voltage stacking to convert high off chip voltage to low on chip voltage at high efficiency. By using a push-pull based switched-capacitor circuit, we are recycling both the current and the current imbalance to reduce power waste. A novel hysteresis-based feedback scheme has been developed to support the switched-capacitor circuit. However, through simulation we have shown how the self regulated stacked domains work best with open loop regulator within certain imbalance constraints. Even with I_{load} varying from 1-10 mA and imbalance between the cores varying up to 50% of I_{load} , 1.2V-0.6V conversion manages to maintain a high efficiency rate of 80-98%. In order to support our claims of improved efficiency for near threshold voltage generation, we have scaled down the design for 0.9V-0.45V conversion with 250uA I_{load} . Simulation results with open-loop regulator showed similar trends of high efficiency (90-95%). Thus with reduction of DC-DC converter energy overhead, just-in-need V_{dd} and near threshold computing can become even more energy efficient.

REFERENCES

- [1] Yu Pu et al, "Misleading Energy and Performance Claims in Sub/Near Threshold Digital Systems" in Proc. Int. Conf. Computer-Aided Design, pp. 625-631, Nov 2010.
- [2] G.Patuonakis et al, "A fully integrated on chip DC-DC conversion and Power Management System", IEEE J. Solid - State Circ., Vol. 39, no. 3, pp 443-451, Mar. 2004.
- [3] K. Mazumdar et al, "Breaking the Power Delivery Wall using Voltage Stacking," Great Lake Symp, May 2012.
- [4] S. Rajapindian et al, "Implicit DC-DC Down conversion through charge-recycling". IEEE J.Solid State Circ., Vol 40, Issue 4, pp 846-852, April 2005.
- [5] Svilen Kanev, "Motivating Software-Driven Current Balancing in Flexible Voltage Stacked Multicore Processors," Master's Thesis, Harvard University, May 2012.
- [6] J Kwong et al, "A 65nm Sub Vt Microcontroller with Integrated SRAM and Switched Capacitor DC-DC Converter," IEEE J.Solid State Circ., vol. 44, pp. 115-126, 2009.