



Cross-layer Accelerated Self-Healing (CLASH)

- Aging Effect in FPGA chips and systems

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BACKGROUND

Circuit reliability

- Defined in term of mean time between failures (MTBF)
- Process, voltage, temperature and aging variations (PVTa) have a substantial effect
- Relatively hard to capture and deal with

Aging Effect

- Deterioration of circuit performance over time
- More significant with extremely scaling technology
- Including bias temperature instability (BTI), Hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), Electromigration (EM), etc.

Purposes

- Capture aging/wearout effect in FPGA based systems
- Develop accelerated recovery mechanism to rejuvenate electronic system
- Develop and optimize aging mechanism models
- Develop aging/wearout sensors for electronic systems

RESEARCH FLOW

Measure FPGA Performance, Power and Variations

Based on evaluation Board (Done)

Design Measurement System

Design connector Board (Done)

Stress FPGA chip

Based on Atmel Board (Ongoing)

Develop recovery strategy

Accelerated and self-heating Thermal recovery (In the future)

Develop aging mechanism models

BTI, HCI and EM models (In the future)

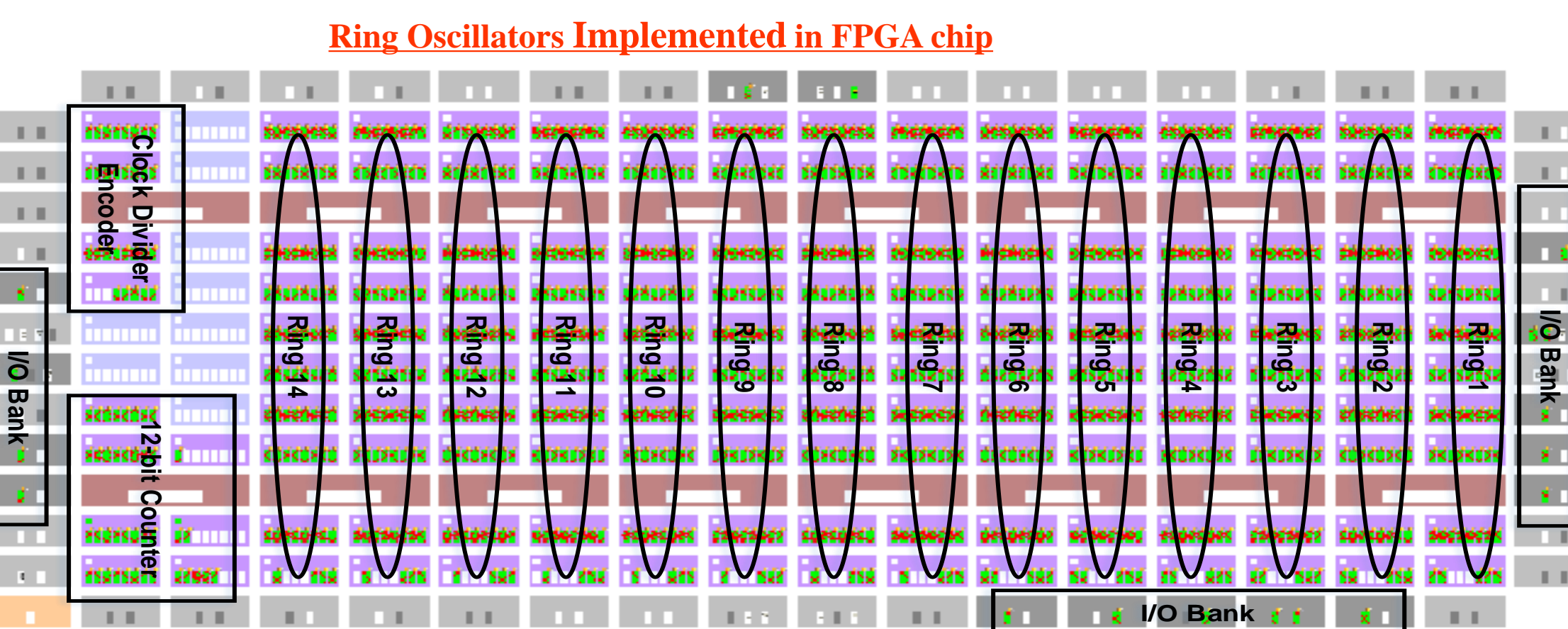
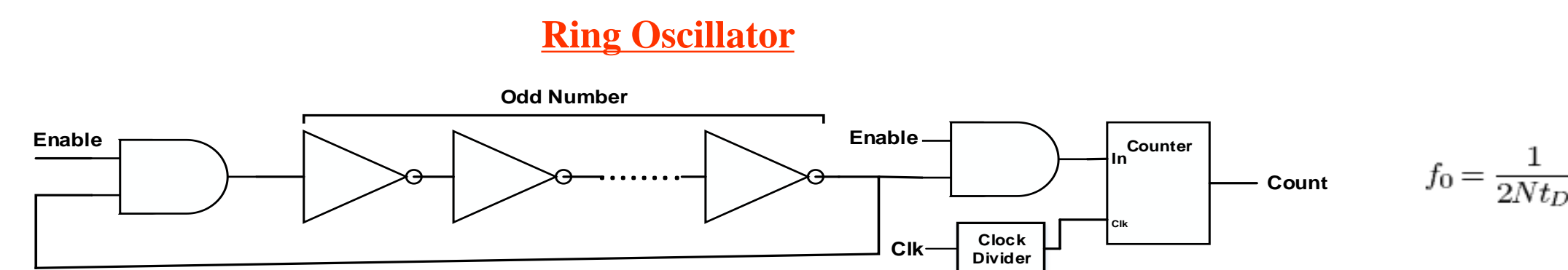
Aging Sensors

Sensing aging effect (In the future)

Validation

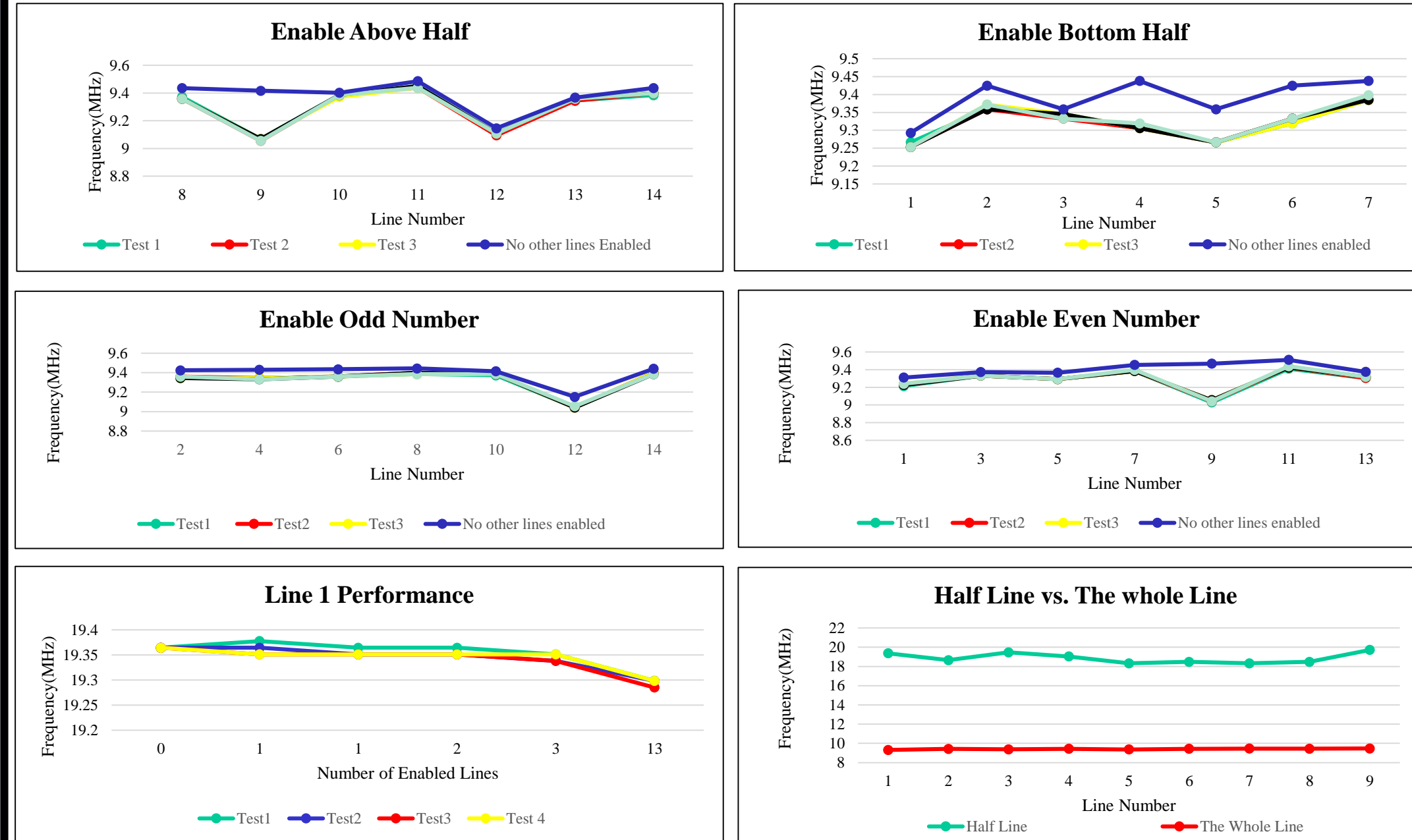
Based on test chip (In the future)

PLATFORM



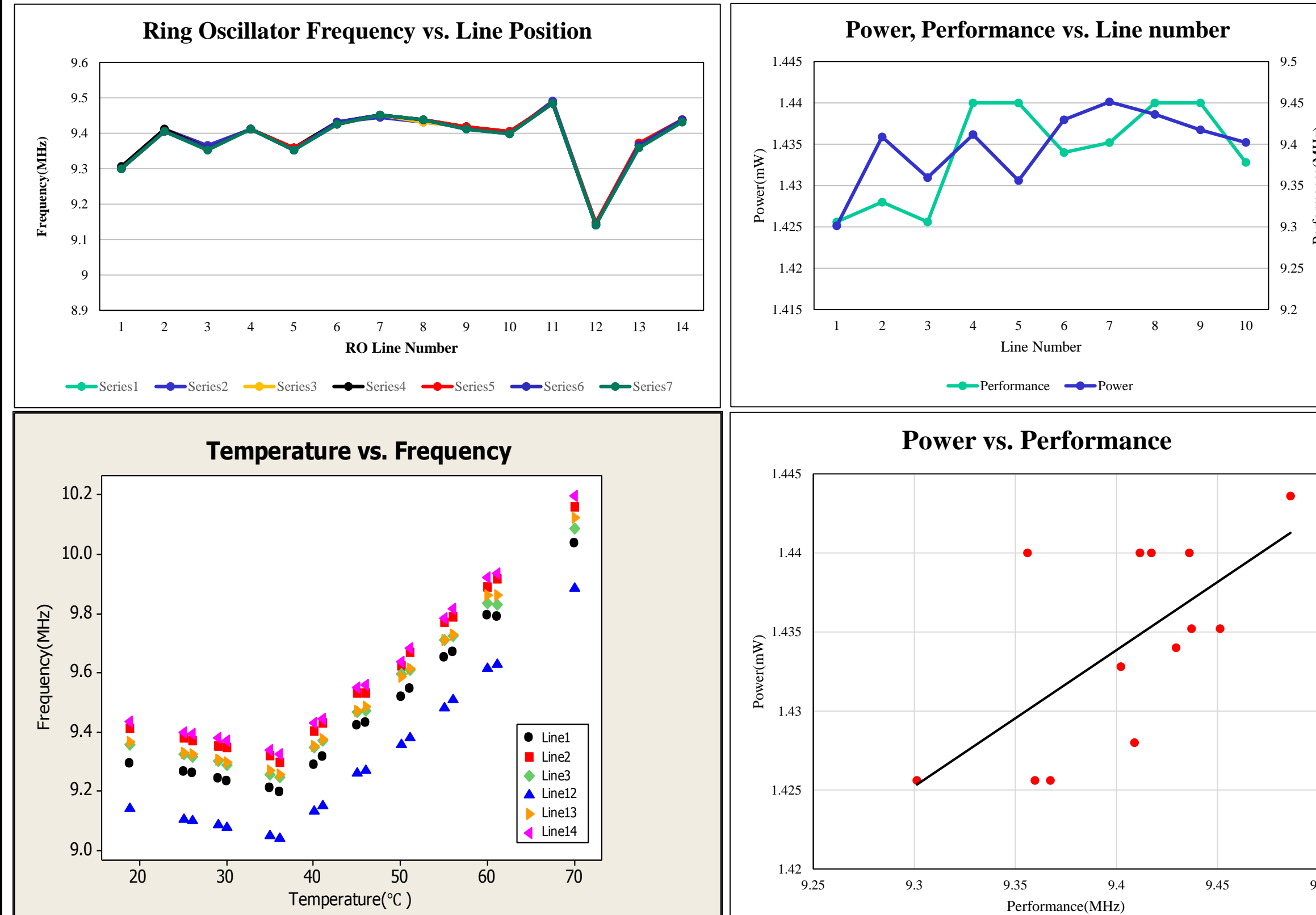
- Each ring oscillator can be enabled separately
- Encoder is used to choose enabled lines
- Clock divider is used to achieve fine granularity
- I/Os are assigned based on availability

MUTUAL EFFECT MEASUREMENTS

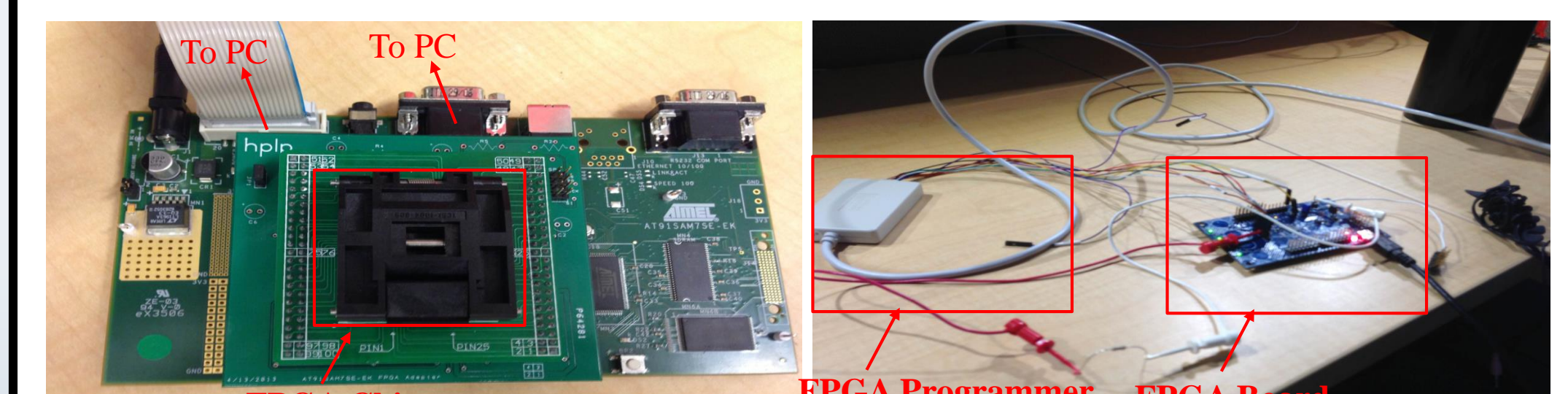


- Mutual effect will affect the performance of ring oscillator
- Self-heating can also influence performance and power

MEASUREMENT RESULTS

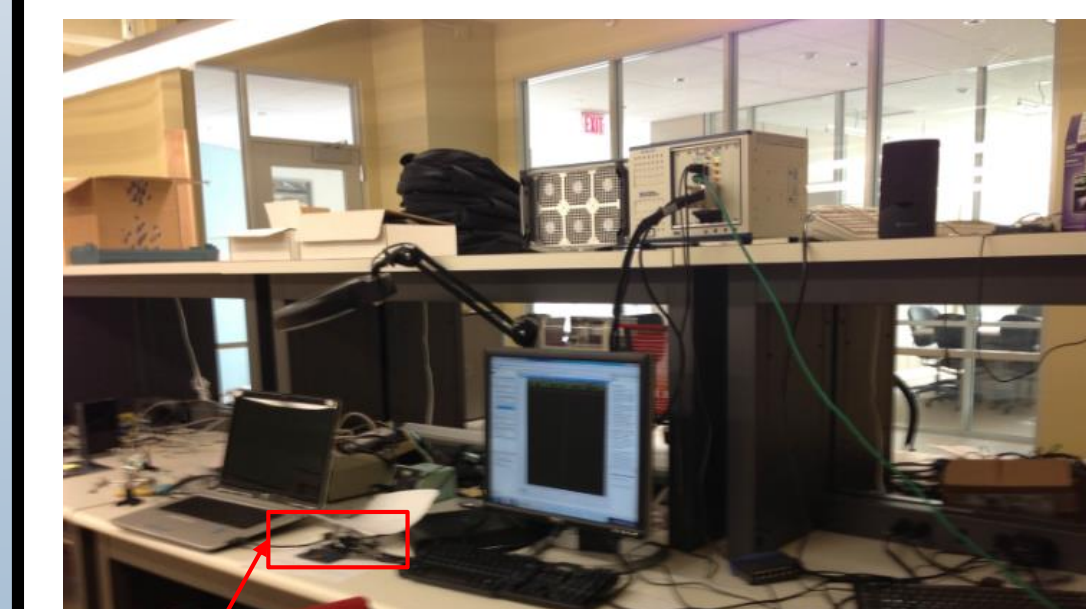


EXPERIMENT SETUP



FPGA Chip
Stress and Recovery System Setup
(Based on AT91SAM7SE-EK)

FPGA Programmer
FPGA Board
Programming FPGA Chip
(Lattice iCE 40 HP1K FPGA)



FPGA Board
Performance measurement with Logic Analyzer



Temperature characteristic measurement
In Thermal Chamber